AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (Currently Amended) An apparatus for use with an adder configured to generate a value and a leading one predictor configured to generate a one hot vector as a leading one prediction ~~corresponding to the value~~ in which each bit of the one hot vector corresponds to a different bit in the value, the apparatus comprising a circuit coupled to receive the value and the ~~leading one prediction, wherein the circuit is configured~~ one hot vector to generate an indication of whether or not the leading one prediction is correct ~~responsive to~~ for the value ~~and the leading one prediction~~.

2. (Currently Amended) The apparatus as recited in claim 1 further comprising a first shifter coupled to receive the value and a shift amount indicated by the leading one prediction, wherein the first shifter is configured to shift the value responsive to the shift amount to produce a shift result~~, and wherein the shifter shifts the value concurrent with the circuit generating the indication~~.

3. (Currently Amended) The apparatus as recited in claim 2 further comprising a second shifter coupled to receive the shift result and the indication, ~~and~~ wherein the second shifter is configured to shift the shift result one bit if the indication indicates that the leading one prediction is not correct.

4. (Canceled)

5. (Currently Amended) The apparatus as recited in claim 4 1 wherein the circuit comprises a plurality of first logic circuits, ~~wherein~~ each of the plurality of first logic circuits is coupled to receive a bit of the value and a corresponding bit of the one hot vector and ~~is configured~~ to generate an output responsive to the bit and the corresponding bit.

6. (Currently Amended) The apparatus as recited in claim 5 further comprising a second logic circuit coupled to receive the outputs of the plurality of first logic circuits and ~~configured~~ to generate the indication responsive to the outputs.

7. (Currently Amended) The apparatus as recited in claim 6 wherein each of the plurality of first logic circuits is an AND gate.

8. (Currently Amended) The apparatus as recited in claim 7 wherein the second logic circuit is configured to OR the outputs of the plurality of first logic circuits.

9. (Original) The apparatus as recited in claim 1 wherein the value is a significand of a floating point number.

10. (Currently Amended) A floating point execution unit comprising:

an adder coupled to receive at least two significands and configured to generate an output significand in response thereto;

a leading one predictor coupled to receive the at least two significands and configured to generate a one hot vector as a leading one prediction in which each bit of the one hot vector corresponds to a different bit in ~~corresponding to~~ the output significand in response to an operation performed on the at least two significands; and

a circuit coupled to receive the output significand and the ~~leading one prediction~~ one hot vector, wherein the circuit is configured to generate an indication of whether or not the leading one prediction is correct ~~responsive to~~ for the output significand ~~and the leading one prediction~~.

11. (Currently Amended) The floating point execution unit as recited in claim 10 further comprising a first shifter coupled to receive the output significand and a shift amount indicated by the leading one prediction, wherein the first shifter is configured to shift the output significand responsive to the shift amount to produce a shift result~~, and wherein the shifter shifts the output significand concurrent with the circuit generating the~~

~~indication~~.

12. (Currently Amended) The floating point execution unit as recited in claim 11 further comprising a second shifter coupled to receive the shift result and the indication, ~~and~~ wherein the second shifter is configured to shift the shift result one bit if the indication indicates that the leading one prediction is not correct.

13. (Canceled)

14. (Currently Amended) The floating point execution unit as recited in claim ~~13~~ 10 wherein the circuit comprises a plurality of first logic circuits, wherein each of the plurality of first logic circuits is coupled to receive a bit of the output significand and a corresponding bit of the one hot vector and ~~is configured~~ to generate an output responsive to the bit and the corresponding bit.

15. (Currently Amended) The floating point execution unit as recited in claim 14 further comprising a second logic circuit coupled to receive the outputs of the plurality of first logic circuits and ~~configured~~ to generate the indication responsive to the outputs.

16. (Currently Amended) The floating point execution unit as recited in claim 15 wherein each of the plurality of first logic circuits is an AND gate.

17. (Original) The floating point execution unit as recited in claim 16 wherein the second logic circuit is configured to OR the outputs of the plurality of logic circuits.

18. (Currently Amended) A method comprising:

receiving a value from an adder and a corresponding leading one prediction in form of a one hot vector in which each bit of the one hot vector corresponds to a different bit in the value; and

determining if the leading one prediction is correct ~~responsive to~~ for the value by using the one hot vector to operate on corresponding bits of the value ~~and the leading one~~

~~prediction~~.

19. (Currently Amended) The method as recited in claim 18 further comprising shifting the value responsive to a shift amount indicated by the leading one prediction to produce a shift result, wherein the shifting is performed concurrent with the determining if the shift amount is correct by the leading one prediction.

20. (Original) The method as recited in claim 19 further shifting the shift result one bit if the leading one prediction is not correct.

21. (Canceled)

22. (Currently Amended) The method as recited in claim ~~21~~ 18 wherein the determining comprises logically ~~combining~~ ANDing each of the bits of the value with a corresponding bit of the one hot vector.

23. (Currently Amended) The method as recited in claim 22 wherein the determining further comprises logically combining a result of the logically ~~combining~~ ANDing each of the bits of the value with the corresponding bit of the one hot vector.

24. (Canceled)

25. (Currently Amended) The method as recited in claim ~~24~~ 22 wherein the logically combining the result comprises logically ORing the result.

26. (Original) The method as recited in claim 18 wherein the value is a significand of a floating point number.